

FIG. 1

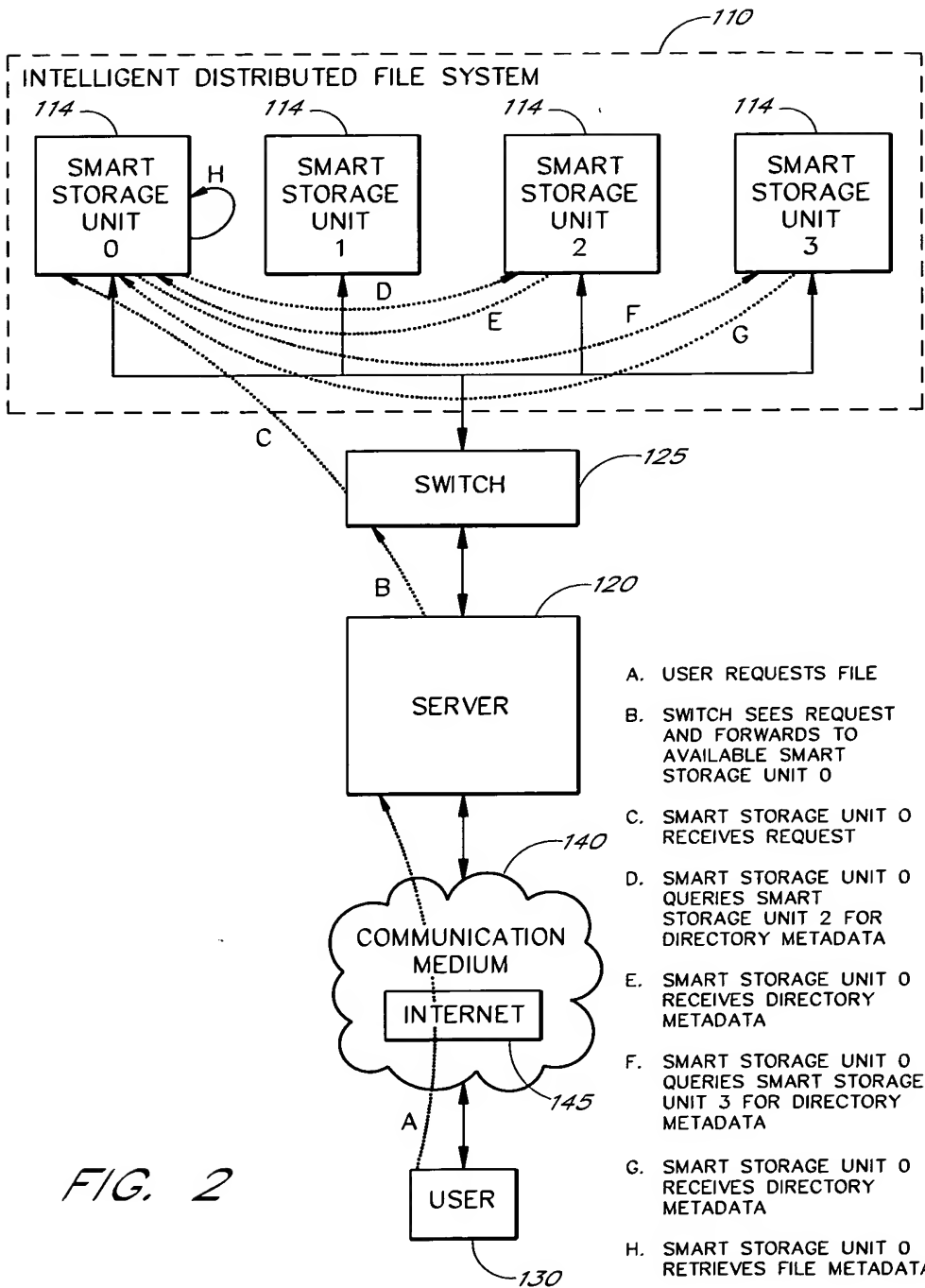


FIG. 2

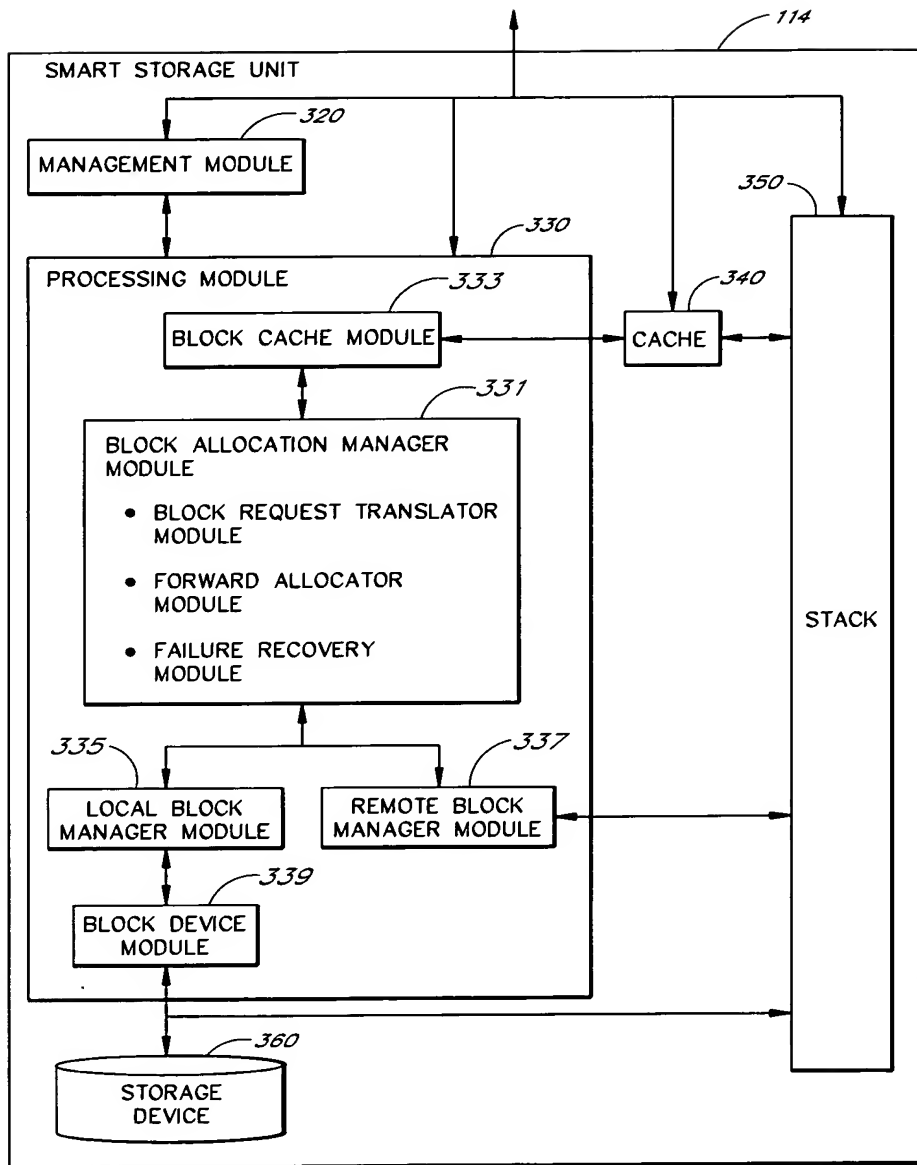


FIG. 3

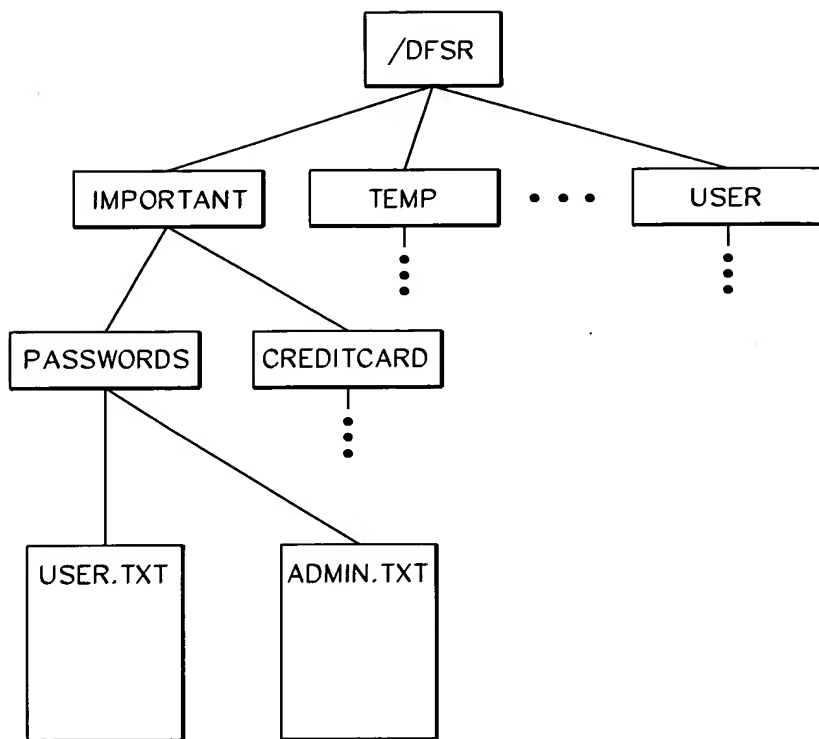


FIG. 4

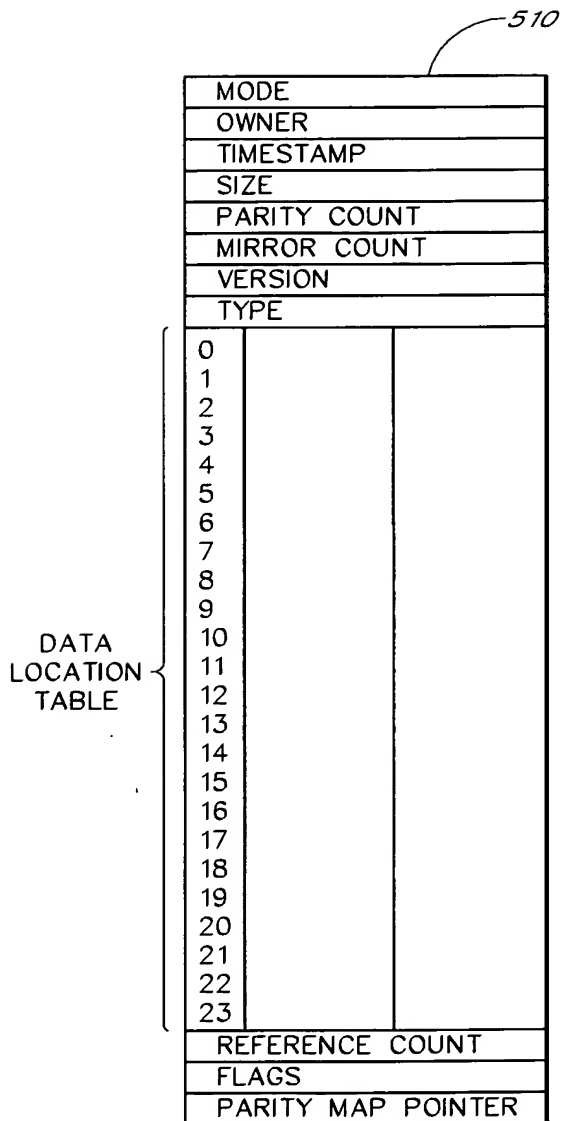


FIG. 5

TYPE 0			
	DEVICE	BLOCK	
0			D0
1			D1
2			D2
3			D3
4			D4
5			D5
6			D6
7			D7
8			D8
9			D9
10			D10
11			D11
12			D12
13			D13
14			D14
15			D15
16			D16
17			D17
18			D18
19			D19
20			D20
21			D21
22			D22
23			D23

FIG. 6A

TYPE 1			
	DEVICE	BLOCK	
0			D0
1			D1
2			D2
3			D3
4			D4
5			D5
6			D6
7			D7
8			D8
9			D9
10			D10
11			D11
12			D12
13			D13
14			D14
15			SI0
16			DI0
17			TI0
18			SI1
19			DI1
20			TI1
21			SI2
22			DI2
23			TI2

FIG. 6B

11
12
13
14
15
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17
18
19
20
21
22
23

TYPE 2

	DEVICE	BLOCK	
0			SI0
1			DI0
2			TI0
3			SI1
4			DI1
5			TI1
6			SI2
7			DI2
8			TI2
9			SI3
10			DI3
11			TI3
12			SI4
13			DI4
14			TI4
15			SI5
16			DI5
17			TI5
18			SI6
19			DI6
20			TI6
21			SI7
22			DI7
23			TI7

FIG. 6C

TYPE 3

	DEVICE	BLOCK	
0			TI0
1			TI1
2			TI2
3			TI3
4			TI4
5			TI5
6			TI6
7			TI7
8			TI8
9			TI9
10			TI10
11			TI11
12			TI12
13			TI13
14			TI14
15			TI15
16			TI16
17			TI17
18			TI18
19			TI19
20			TI20
21			TI21
22			TI22
23			TI23

FIG. 6D

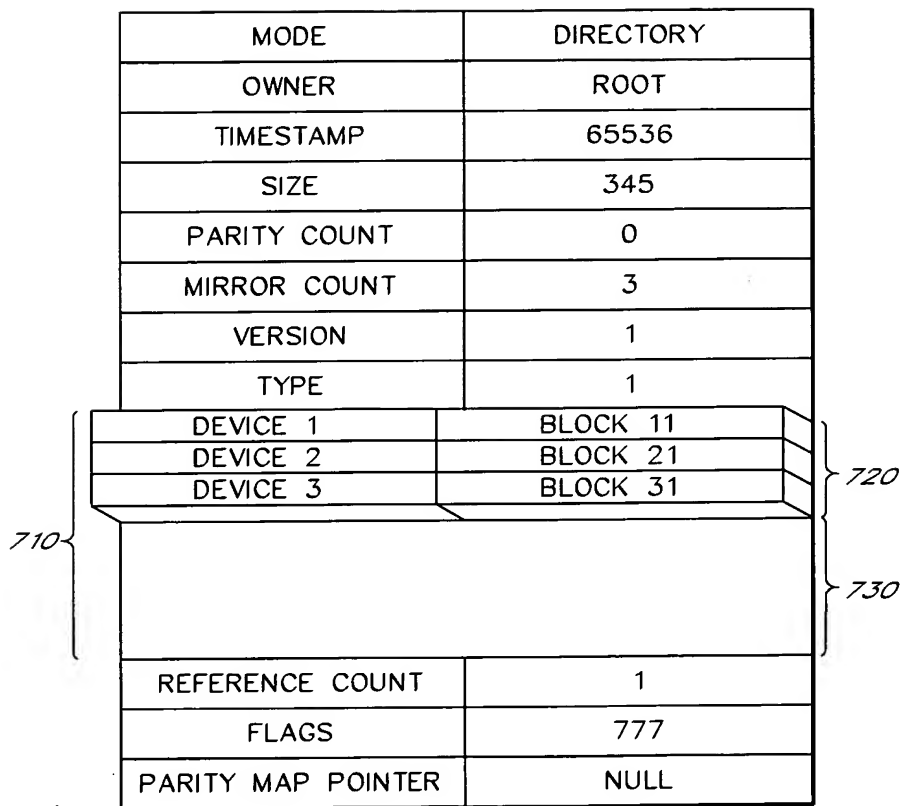


FIG. 7A

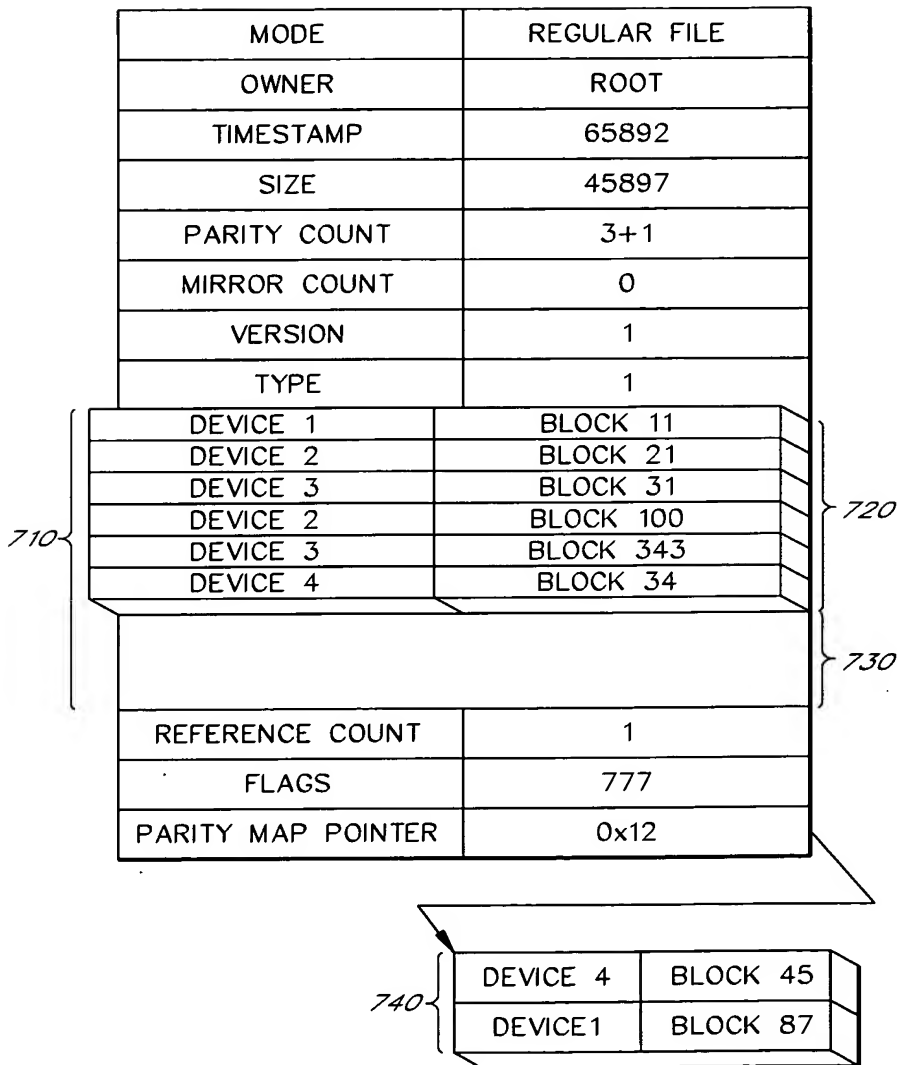


FIG. 7B

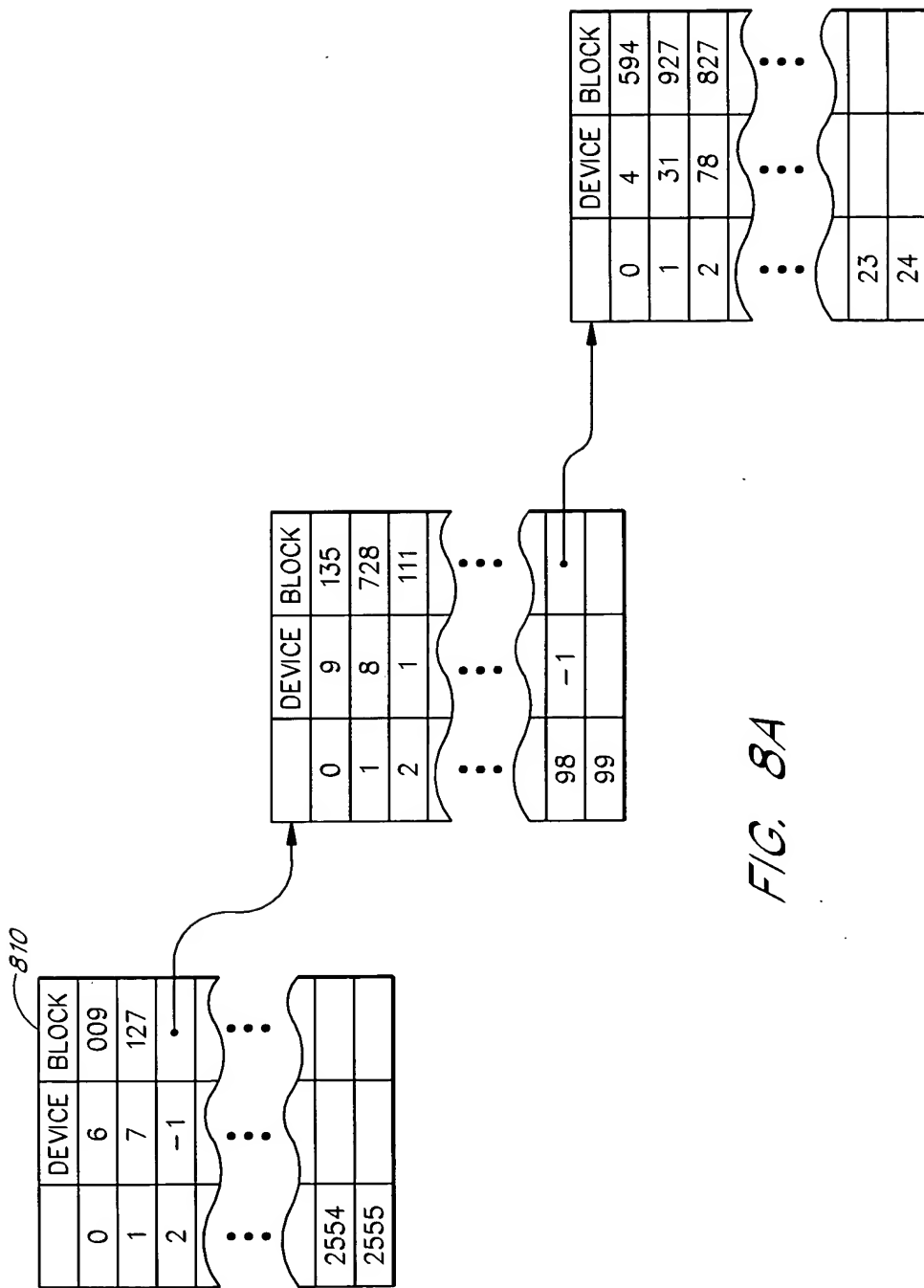


FIG. 8A

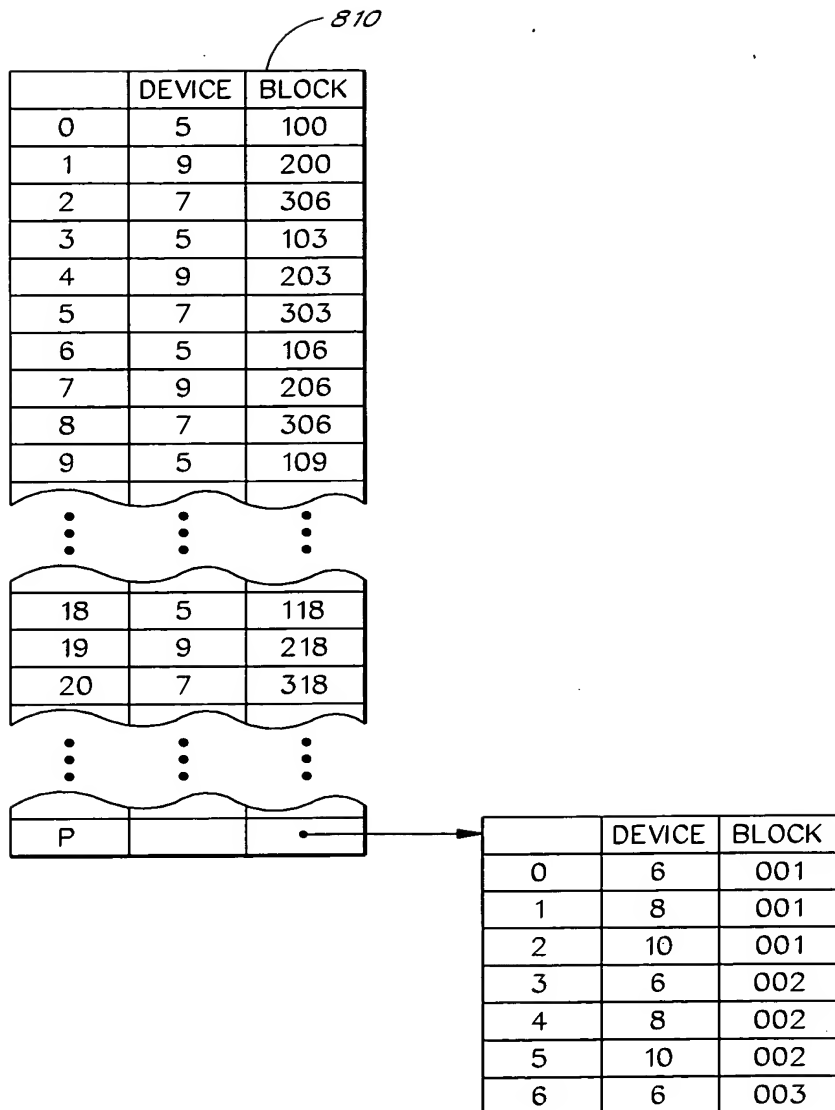
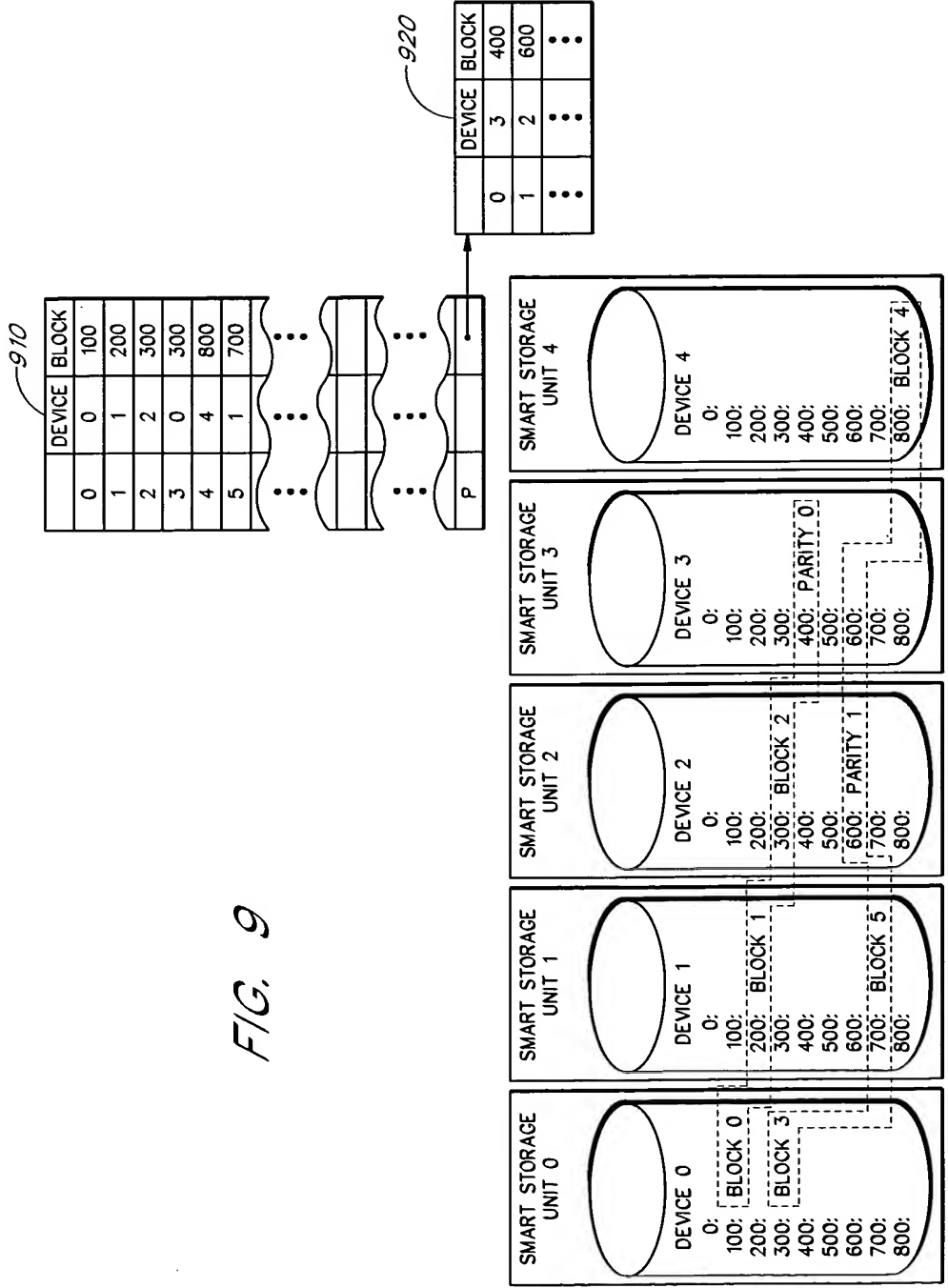


FIG. 8C

FIG. 9



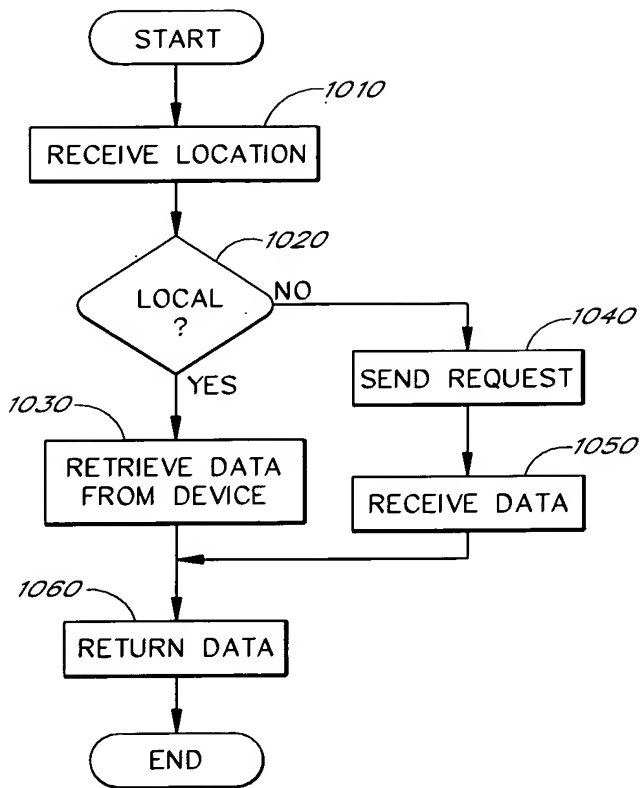


FIG. 10

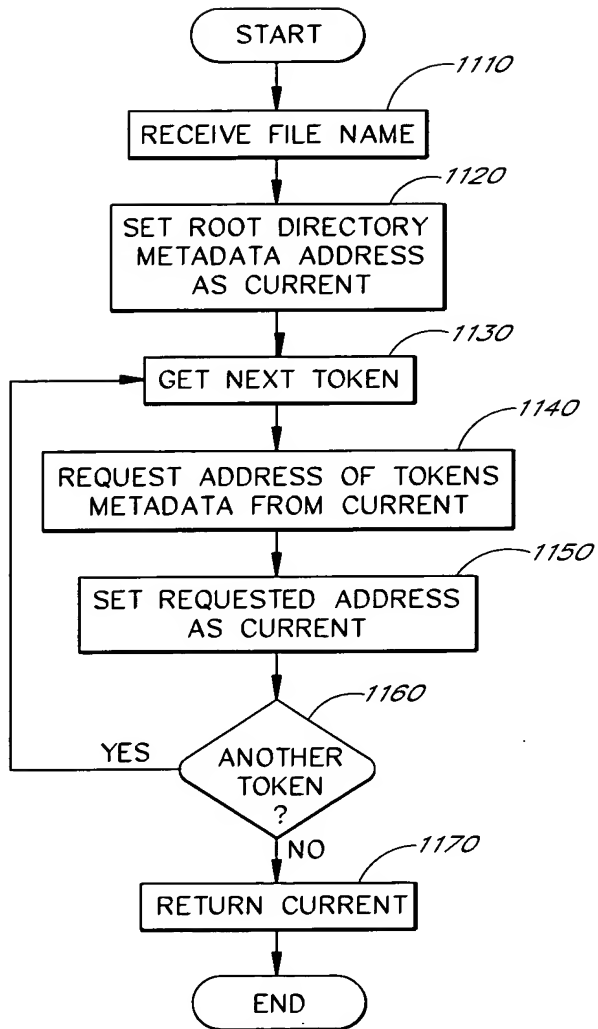


FIG. 11

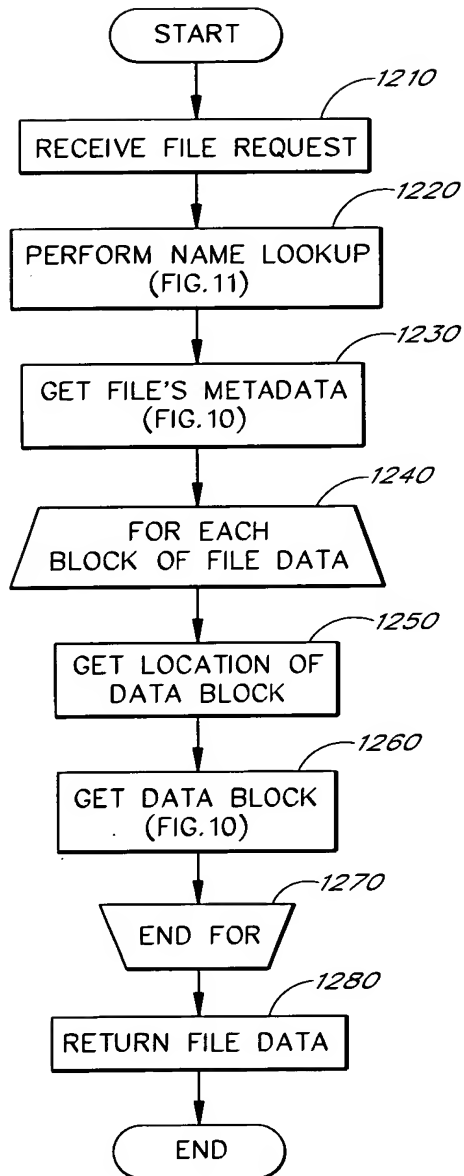


FIG. 12

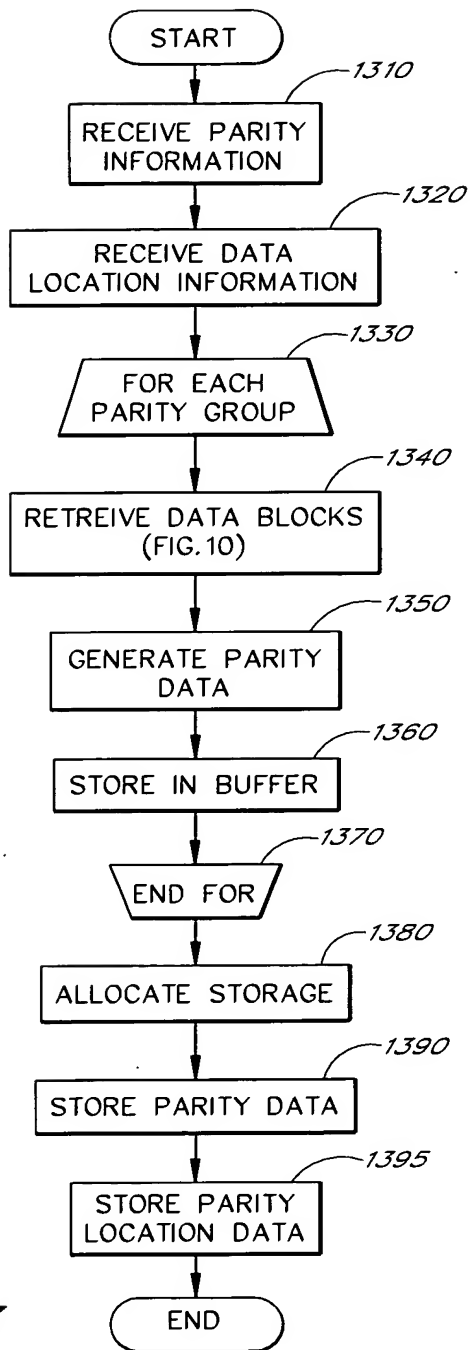


FIG. 13

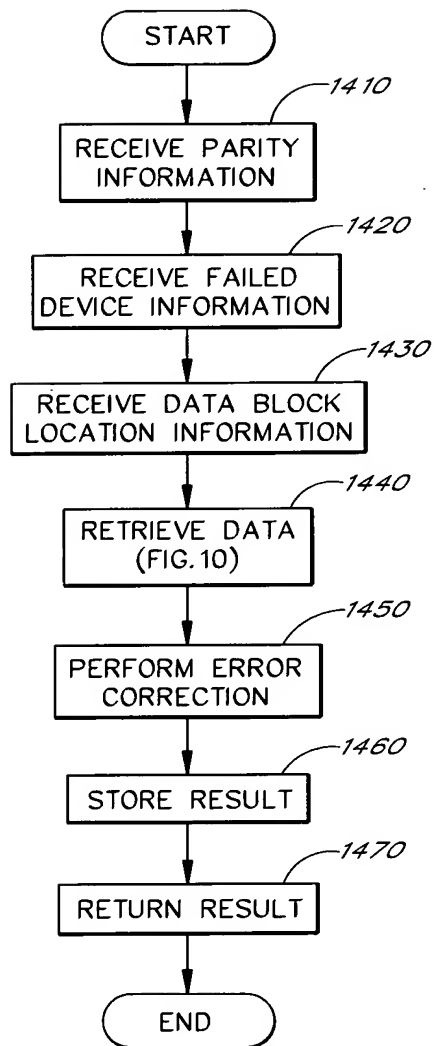


FIG. 14